REMARKS

The Examiner is thanked for the thorough examination of the present application. The Office Action, however, tentatively rejected all claims 1-20 under 35 U.S.C. § 102(b) as allegedly anticipated by U.S. patent 5,964,859 to Steinbach. Applicants amend the application herein to clearly define over the cited art. Specifically, Applicants have amended independent claim 1 to incorporate the subject matter of claim 2. Applicants have likewise amended independent claim 6 to incorporate the subject matter of claim 7. Applicants have also amended independent claim 19 to incorporate the subject matter of claim 20. Finally, Applicant have canceled claims 2, 7, and 20, and amended claims 3, 4, 8, and 9 to revise their dependencies. Applicants respectfully submit that the rejections be reconsidered and withdrawn for at least the reasons set forth herein.

Independent Claim 1

The Office Action rejected claim 2 (now incorporated into claim 1) under 35 U.S.C. § 102(b) as allegedly anticipated by Steinbach. Applicants respectfully request reconsideration for at least the following reasons.

Claim 1, as amended, recites:

> 1. A method comprising:
> determining at least one characteristic of a first input/output (I/O) device that is coupled to a memory device interface, the memory device interface being configured to enable data transfers between the I/O device and a memory device;
> buffering data corresponding to the first I/O device in a first portion of a buffer of the memory device interface, a size of the first portion being responsive to the at least one characteristic of the first I/O device;
> ***determining at least one characteristic of a second I/O device that is coupled to the memory device interface; and***

> ***buffering data corresponding to the second I/O device in a second portion of the buffer, a size of the second portion being responsive to the at least one characteristic of the second I/O device.***

(*Emphasis added.*) Claim 1 patently defines over the cited art for at least the reason that Steinbach fails to disclose the features emphasized above.

The Office Action cited col. 3 line 53 through col. 4 line 6 as disclosing the features emphasized above. In fact, the Office Action cited this same portion of Steinbach as disclosing both the claimed buffering of the first I/O device and the claimed buffering of the second I/O device. This portion of Steinbach actually states:

> The present invention still further contemplates a bus bridge. The bus bridge includes a first bus interface, a second bus interface, a buffer pool, and a buffer pool control unit. The first bus interface is adapted to receive control, address, and data signals from a first bus device connected to a first bus. The second bus interface is adapted to receive control, address, and data signals from a second bus device connected to a second bus. The buffer pool includes a plurality of storage buffers. The buffer pool control unit is adapted to receive the information from the first and second bus interfaces and is further adapted to temporarily allocate each of the plurality of storage buffers as either a fetch buffer or a post buffer in response to the information from the first and second bus interfaces. Preferably, each of the plurality of storage buffer locations includes corresponding tag information for identifying an originating or destination location within a system main memory of the data stored in the storage buffer. Each of the storage buffers preferably includes corresponding allocation information used by the buffer pool control unit for the temporary allocation of the storage buffers.

As can be readily verified, Steinbach discloses a bridge between two busses. The bridge includes a buffer pool, which comprises buffers that can store information from each of the busses. Significantly, however, the buffer pool of Steinbach does not disclose the separate buffering of information from both a first I/O device and a second I/O device, such that the buffering of each I/O device is performed such that a size of the respective buffering portions (or separate buffers of the buffer pool) is determined by characteristics of the I/O devices.

Simply stated, there are no such comparable teachings in Steinbach to anticipate the features that are expressly recited in claim 1. For at least this reason, the rejection should be withdrawn.

Claims 3-5 depend from claim 1, and therefore patently define over the cited art for at least the same reason.

Independent Claim 6

The Office Action rejected claim 7 (now incorporated into claim 6) under 35 U.S.C. § 102(b) as allegedly anticipated by Steinbach. Applicants respectfully request reconsideration for at least the following reasons.

Claim 6, as amended, recites:

> 6. A method for allocating buffer capacity in a memory device interface that is configured to transfer data between an input/output (I/O) device and a memory device, the method comprising:
> buffering data received via a first data transfer link in a first portion of a buffer of the memory device interface;
> buffering data received via a second data transfer link in a second portion of the buffer, a buffering capacity of the first portion being different than a buffering capacity of the second portion; and
> ***wherein the buffering capacity of the first portion is responsive to at least one characteristic of a first I/O device that provides data to the memory device interface via the first data transfer link, and the buffering capacity of the second portion is responsive to at least one characteristic of a second I/O device that provides data to the memory device interface via the second data transfer link.***

(*Emphasis added.*) Claim 6 patently defines over the cited art for at least the reason that Steinbach fails to disclose the features emphasized above.

The Office Action cited the same portion of Steinbach as allegedly disclosing the feature of claim 7 as it cited in rejecting claim 1 (previously embodied in claim 2) discussed above. As noted above, the Office Action cited the same portion of Steinbach as disclosing the features of

the buffering of the first I/O device and the buffering of the second I/O device. However, Steinbach does not disclose separate I/O devices. Further, Steinbach does not disclose that the "buffering capacity of the first portion is responsive to at least one characteristic of a first I/O device that provides data to the memory device interface via the first data transfer link, and the buffering capacity of the second portion is responsive to at least one characteristic of a second I/O device that provides data to the memory device interface via the second data transfer link." For at least this reason, the rejection of claim 6 should be withdrawn.

Claims 8 and 9 each depend from claim 6 and therefore patently define over Steinbach for at least the same reasons.

Independent Claims 10 and 15

The Office Action rejected independent claims 10 and 15 on the same basis as claim 1. For at least the reasons set forth below, Applicants disagree and request reconsideration of the rejections.

Claim 10 and 15 recite:

10. A memory device interface that is configured to enable data transfers between an input/output (I/O) device, the memory device interface comprising:
a buffer;
a first plurality of registers that are configured to enable the memory device interface to buffer in a first portion of the buffer data corresponding to a first I/O device; and
a second plurality of registers that are configured to enable the memory device interface to buffer in a second portion of the buffer data corresponding to a second I/O device, a size of the first portion of the buffer being different than a size of the second portion of the buffer.

15. A memory device interface comprising:
a buffer;
a first plurality of registers that are configured to enable the memory device interface to buffer in a first portion of the buffer data received via a first

data transfer link; and

a second plurality of registers that are configured to enable the memory device interface to buffer in a second portion of the buffer data received via a second data transfer link, a size of the first portion of the buffer being different than a size of the second portion of the buffer.

(*Emphasis added.*) Claims 10 and 15 patently define over the cited art for at least the reason that Steinbach fails to disclose the features emphasized above.

Specifically, as emphasized above, claims 10 and 15 define, among other features, "a second plurality of registers that are configured to enable the memory device interface to buffer in a second portion of the buffer data corresponding to a second I/O device, a size of the first portion of the buffer being different than a size of the second portion of the buffer." The rejection of these claims (set forth in the Office Action) alleges that Steinbach discloses "a size of the first portion being responsive to the at least one characteristic of the first I/O device." (Office Action, p. 2, last 3 lines of paragraph 3).

Even assuming, for the sake of argument, that Steinbach teaches what the Office Action alleges it teaches, there is still no allegation in the Office Action of "***a size of the first portion of the buffer being different than a size of the second portion of the buffer.***" For at least this reason, the rejection of independent claims 10 and 15 is deficient and should be withdrawn.

In addition to the foregoing distinction, claims 10 and 15 define both a first and a second plurality of registers that are configured to enable a memory device to interface with and buffer data in first and second portions of the buffer. This claimed feature is neither taught nor suggested in Steinbach.

For at least the foregoing reasons, the rejections of independent claims 10 and 15 should be withdrawn. For at least the same reasons, dependent claims 11-14 and 16-18 patently define over the cited art.

Independent Claim 19

The Office Action rejected claim 20 (now incorporated into claim 19) under 35 U.S.C. § 102(b) as allegedly anticipated by Steinbach, on the same basis that the Office Action rejected claim 2. Claim 19 defines features that loosely parallel the claimed features of claim 1 (with the features of claim 19 being set forth in means-plus-function format).

Specifically, claim 19 recites:

> 19. A system comprising:
> means for determining at least one characteristic of a first input/output (I/O) device that is coupled to a memory device interface, the memory device interface being configured to enable data transfers between the I/O device and a memory device;
> means for buffering data corresponding to the first I/O device in a first portion of a buffer of the memory device interface, a size of the first portion being responsive to the at least one characteristic of the first I/O device;
> ***means for determining at least one characteristic of a second I/O device that is coupled to the memory device interface; and***
> ***means for buffering data corresponding to the second I/O device in a second portion of the buffer, a size of the second portion being responsive to the at least one characteristic of the second I/O device.***

(*Emphasis added.*) Claim 19 patently defines over the cited art for at least the reason that Steinbach fails to disclose the features emphasized above.

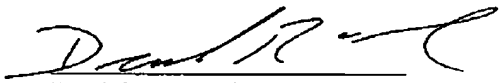
As claim 19 defines elements that loosely correspond to the element of claim 1, and as claim 19 stands rejected on the same bases as claim 1, Applicants respectfully submit that the rejection of claim 19 should be withdrawn for the same reasons set forth above in connection with claim 1.

CONCLUSION

In view of the foregoing, it is believed that all pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

No fees are believed to be due in connection with this amendment and response. If, however, any fees are deemed to be payable, you are hereby authorized to charge any such fees to Hewlett-Packard Company's deposit account No. 08-2025.

Respectfully submitted,



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